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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RUTTEN, JAMES D	
ART UNIT	PAPER NUMBER
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,651	SHAPIRO, MICHAEL W.	
	Examiner	Art Unit	
	J. Derek Rutten	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 have been examined.

Specification

2. The spacing of the lines on pages 6-7 (i.e., table 1) of the specification is such as to make reading difficult. New application papers with lines 1½ or double spaced on good quality paper are required.

Claim Objections

3. Claim 10 is objected to because of the following informalities: Line 2 contains the phrase "an opcode bits" which should be --*that* opcode bits--. Similarly, in line 3 the phrase "the opcode bit is" should be --the opcode bits are--. Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1, 2, 6-9, and 22-35 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

6. Claims 1, 2, 6-9 and 19 are directed to "a method for protecting byte code." This claimed subject matter lacks a practical application since it fails to produce a useful, concrete and tangible result. Specifically, the claimed subject matter does not produce a useful result because the claimed subject matter fails to sufficiently reflect at least one practical utility set forth in the

descriptive portion of the specification. More specifically, while the described practical utility is directed to protecting byte code, the claimed subject matter (see claim 1) relates ONLY to validating and performing a safety check which merely evaluates a control transfer.

7. Claims 22-35 are directed to "a mechanism." This mechanism is interpreted in accordance with paragraph [0017] in the specification as being a software mechanism (e.g., "a virtual machine interpreter"), which can be classified as descriptive material. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. Data structures not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1, 2, 6-9 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 is directed to "a method for protecting byte code." However, the method steps merely involve "validating...and performing at least one safety check." The intended function as stated in the preamble is not distinctly claimed. In contrast, claim 3 recites: "rejecting the tracing program if the byte code is not validated as safe." This step provide the protecting step indicated in the preamble. Claims 2 and 6-9 are rejected as being dependent upon a rejected base claim.

11. Claim 21 recites:

> *evaluating an effective address of the store operation against a list of pre-computed address ranges assigned by the virtual machine to the tracing program; and*
> *aborting execution of the virtual machine emulation if the effective address falls within the list of pre-computed address ranges.*

These two steps are at odds with each other. The evaluating step provides an address space for the tracing program. However, the aborting step does not allow the tracing program to use the address space. This presents a situation where the program could not execute since it would be unable to use the addresses provided by the virtual machine. Further, this is at odds with paragraph [0030] of the specification:

> Lastly, for any store instruction, a mechanism is provided whereby the effective address is checked against a list of pre-computed address ranges assigned by the virtual machine to the tracing program. If the effective address does not fall within any of these ranges, emulation is aborted and no store instruction is issued.

Note that in the description in the specification, emulation is aborted if the address does *not* fall within the range, whereas in the claim, emulation is aborted if it *does* fall within the range. For the purpose of further examination, this claim will be interpreted according to the description in the specification.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-6, 8-11, 13, 14, 19, 22, 23, 25-28, 30, 31 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,668,999 to Gosling (hereinafter "Gosling") in view of U.S. Patent No. 6,581,206 to Chen (hereinafter "Chen") in view of in view of U.S. Patent No. 6,026,237 to Berry et al. (hereinafter "Berry").

In regard to claim 1, Gosling discloses:

A method for protecting a byte code ... (e.g., see Figure 4A), *comprising:*

...

performing at least one safety check while executing the plurality of instructions during a virtual machine emulation, See Gosling column 5 lines 22-55 for a discussion of a bytecode verifier that performs safety checks using a "virtual stack," i.e. emulator.

wherein the at least one safety check evaluates for a control transfer to an earlier instruction in the byte code sequence. See column 8 lines 4-5, e.g. "backward jump."

Gosling does not expressly disclose: *validating a plurality of instructions when loading the byte code;* However, Chen teaches bytecode validation. See column 7 lines 24-26, e.g. "validating the bytecode." It would have been obvious to one of ordinary skill

in the art at the time the invention was made to use Chen's validation with Gosling's verification in order to prevent erroneous program execution (see Chen column 3 lines 50-58).

Gosling and Chen do not expressly disclose *a tracing framework.* However, Berry teaches the use of a tracing framework to execute tracing programs. See column 5 lines 51-54, e.g. "a trace hook." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Berry's tracing with Gosling's bytecode in order to measure the performance of a Java® application (see Berry column 2 lines 7-9).

In regard to claim 2, the above rejection of claim 1 is incorporated. Gosling does not expressly disclose: *obtaining a tracing program comprising the plurality of instructions*. However, Berry teaches the use of a tracing framework to execute tracing programs. See column 5 lines 51-54, e.g. "a trace hook." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Berry's tracing with Gosling's bytecode in order to measure the performance of a Java® application (see Berry column 2 lines 7-9).

In regard to claim 3, the above rejection of claim 2 is incorporated. Chen further discloses: *rejecting the tracing program if the byte code is not validated as safe.* See column 7 lines 40-42.

In regard to claim 4, the above rejection of claim 1 is incorporated. Gosling further discloses: *reporting an error condition and aborting the virtual machine emulation if an unsafe instruction is detected.* See column 8 lines 46-52.

In regard to claim 5, the above rejection of claim 1 is incorporated. Gosling further discloses: *completing the virtual machine emulation if a safe instruction is detected.* See column 8 lines 30-34.

In regard to claim 6, the above rejection of claim 1 is incorporated. Gosling further discloses: *wherein the transfer comprises one selected from the group consisting of a direct control transfer and indirect control transfer.* See column 6 lines 42-44, e.g. "absolute or relative address."

In regard to claim 8, the above rejection of claim 1 is incorporated. Gosling further discloses: *wherein the byte code comprises an instruction set of a virtual machine.* See column 3 lines 27-28, e.g. "instruction set," and column 4 line 42, e.g. "bytecode interpreter."

In regard to claim 9, the above rejection of claim 8 is incorporated. Gosling further discloses: *wherein the instruction set comprises at least one selected from the group consisting of an arithmetic operation, a logical operation, a load operation, a store operation, and a control transfer operation.* See table 1.

In regard to claim 10, the above rejection of claim 2 is incorporated. Gosling does not expressly disclose validating. However, Chen further teaches: *wherein the validating the plurality of instructions comprises: verifying [that] opcode bits identify a*

valid operation; and rejecting the tracing program if the opcode [bits are] invalid. See column 7 lines 40-42, e.g. "bytecode is not supported."

In regard to claim 11, the above rejection of claim 2 is incorporated. Gosling does not expressly disclose validating. However, Chen further teaches: *wherein the validating the plurality of instructions comprises: rejecting the tracing program if an operand name does not refer to a valid operand provided by the virtual machine emulation.* See column 7 lines 40-42, e.g. "unsupported types."

In regard to claim 13, the above rejection of claim 2 is incorporated. Gosling does not expressly disclose validating. However, Chen further discloses: *wherein the validating the plurality of instructions comprises: determining whether a subroutine is valid, when one of the plurality of instructions invokes a named subroutine; and rejecting the tracing program if the subroutine is invalid.* See column 6 lines 62-64, e.g. "method declaration is supported."

In regard to claim 14, the above rejection of claim 2 is incorporated. Gosling does not expressly disclose validating. However, Chen further discloses: *wherein the validating the plurality of instructions comprises: summing a total number of the plurality of instructions in the input byte code stream; and rejecting the tracing program if the total number exceeds a user-configurable limit.* See column 9 lines 5-10.

In regard to claim 19, the above rejection of claim 9 is incorporated. Gosling further discloses: *wherein the performing the at least one safety check comprises: evaluating an effective address of the load or store operation for validity prior to executing the load operation.* See column 4 lines 48-53 and column 13 line 36, e.g.

"iload." Note that there is no provision in the claim language for evaluation of an address prior to execution of a store operation.

In regard to claim 22, all limitations have been addressed in the above rejection of claim 1.

In regard to claims 23, 25-28, 30 and 31, the above rejection of claim 22 is incorporated. All further limitations have been addressed in the above rejection of claims 6, 8-11, 13 and 14, respectively.

In regard to claim 36, Gosling discloses: *A computer system for protecting a byte code ..., comprising: a processor; a memory; a storage device; and software instructions stored in the memory.* See Figure 1, e.g. "CPU 106," "RAM 110," "Disc 112," and "Downloaded Program 103." All further limitations have been addressed in the above rejection of claim 1.

In regard to claims 37-41, the above rejection of claim 36 is incorporated. All further limitations have been addressed in the above rejection of claims 2-6, respectively.

14. Claims 7 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosling, Chen and Berry as applied to claims 1 and 22 above, and further in view of "Compilers: Principles, Techniques, and Tools" by Aho et al. (hereinafter "Aho").

In regard to claim 7, the above rejection of claim 1 is incorporated. Gosling, Chen and Berry do not expressly disclose: *wherein the validating occurs during a single pass over the plurality of instructions.* However, Aho teaches single pass analysis over a

plurality of instructions. See bottom of page 279, e.g. "single pass." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Aho's teaching of single pass with Chen's validating in order to provide efficiency (see Aho, last line on page 279).

In regard to claim 24, the above rejection of claim 22 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

15. Claims 12, 21 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosling, Chen and Berry as applied to claim 9 above, and further in view of "Java Bytecode Verification: Algorithms and Formalizations" by Leroy (hereinafter "Leroy").

In regard to claim 12, the above rejection of claim 2 is incorporated. Gosling, Chen and Berry do not expressly disclose: *wherein the validating the plurality of instructions comprises: computing a destination location within an instruction stream from one of the plurality of instructions; and rejecting the tracing program if the destination location is invalid.* However, Leroy teaches that bounds checking needs to be performed for arrays. See last paragraph of section 2, appearing on page 238, e.g. "array bounds checks." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Leroy's teaching of bounds checks with Gosling's verification in order to ensure that crucial properties are checked (see Leroy, last paragraph of section 2).

In regard to claim 21, the above rejection of claim 9 is incorporated. Gosling discloses *a list of pre-computed address ranges assigned by the virtual machine... and aborting execution of the virtual machine emulation* See column 11 lines 10-12 and column 14 line 20, e.g. "newarray." Gosling, Chen and Berry do not expressly disclose: *wherein the performing the at least one safety check comprises: evaluating an effective address of the store operation against a list of pre-computed address ranges assigned by the virtual machine to the tracing program; and aborting execution of the virtual machine emulation if the effective address [does not] falls within the list of pre-computed address ranges*. However, Leroy teaches that bounds checking needs to be performed for arrays. See last paragraph of section 2, appearing on page 238, e.g. "array bounds checks." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Leroy's teaching of bounds checks with Gosling's verification in order to ensure that crucial properties are checked (see Leroy, last paragraph of section 2).

In regard to claim 29, the above rejection of claim 22 is incorporated. All further limitations have been addressed in the above rejection of claim 12.

16. Claims 15 and 32 rejected under 35 U.S.C. 103(a) as being unpatentable over Gosling, Chen and Berry as applied to claims 9 and 26 above, and further in view of U.S. Patent 5,432,795 to Robinson (hereinafter "Robinson").

In regard to claim 15, the above rejection of claim 9 is incorporated. Gosling discloses overflow verification and aborting execution. See column 2 lines 1-7 and column 11 lines 10-12. Gosling, Chen and Berry do not expressly disclose: *wherein the performing the at least one safety check comprises: evaluating whether an arithmetic operation results in a processor exception; and aborting execution of a tracing program if any exception conditions result.* However, Robinson teaches arithmetic exceptions including overflow faults. See column 11 lines 67-68, e.g. "overflow faults." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Robinson's teaching of arithmetic exceptions with Gosling's overflow verification in order to prevent the use of programs that promote overflow faults (see Gosling column 2 lines 6-7).

In regard to claim 32, the above rejection of claim 26 is incorporated. All further limitations have been addressed in the above rejection of claim 15.

17. Claims 16-18 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosling, Chen and Berry as applied to claims 9 and 26 above, and further in view of U.S. Patent 6,125,441 to Green (hereinafter "Green").

In regard to claim 16, the above rejection of claim 9 is incorporated. Gosling further discloses: *wherein the performing the at least one safety check comprises: evaluating an effective address of the load operation; and aborting execution of the tracing program if ... improper;* See column 4 lines 48-53, column 11 lines 10-12 and

column 13 line 36, e.g. "iload." Gosling, Chen and Berry do not expressly disclose: *determining an appropriate alignment for the effective address*. However, Green teaches that verification involves instruction alignment. See column 12 lines 6-22, e.g. "quick verification." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Green's alignment verification with Gosling's load operation in order to ensure proper decoding of an instruction (see Green column 1 line 66 – column 2 line 2).

In regard to claim 17, the above rejection of claim 9 is incorporated. Gosling further discloses: *wherein the performing the at least one safety check comprises: evaluating an effective address of the load operation before issuing the underlying instructions; and aborting execution of the tracing program if ... improper* See column 4 lines 48-53, column 11 lines 10-12 and column 13 line 36, e.g. "iload." Note that instruction issuance does not occur before actual execution. All further limitations have been addressed in the above rejection of claim 16.

In regard to claim 18, the above rejection of claim 9 is incorporated. Gosling further discloses: *wherein the performing the at least one safety check comprises: evaluating an effective address of the store operation before issuing the underlying instructions; ... and aborting execution of the tracing program if ... improper.* See column 4 lines 48-53, column 11 lines 10-12 and column 13 line 47, e.g. "istore." All further limitations have been addressed in the above rejection of claim 16.

In regard to claims 33-35, the above rejection of claim 26 is incorporated. All further limitations have been addressed in the above rejection of claims 16-18, respectively.

18. ClaimXXX rejected under 35 U.S.C. 103(a) as being unpatentable over Gosling, Chen and Berry as applied to claim 9 above, and further in view of U.S. Patent 4,713,749 to Magar et al. (hereinafter "Magar").

In regard to claim 20, the above rejection of claim 9 is incorporated. Gosling further discloses: *wherein the performing the at least one safety check comprises: evaluating an effective address of the load or store operation; and aborting execution of the virtual machine emulation.* See column 4 lines 48-53, column 11 lines 10-12 and column 13 line 36, e.g. "iload." Gosling, Chen and Berry do not expressly disclose: *against a list of pre-computed address ranges assigned to a memory-mapped device hardware state;* or *if the effective address falls within the list of pre-computed address ranges.* However, Magar teaches the evaluation of memory-mapped registers. See column 36 lines 32-36. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Magar's teaching of memory mapped addresses with Gosling's verification in order to avoid using reserved locations for storage (see Magar column 36 lines 35-36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571)272-3703. The examiner can normally be reached on T-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jdr

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